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TITLE: CIRCUIT AND METHOD FOR ENHANCED LOW FREQUENCY SWITCHING NOISE SUPPRESSION IN MULTILAYER PRINTED CIRCUIT BOARDS USING A CHIP CAPACITOR LATTICE

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CIRCUIT AND METHOD FOR ENHANCED LOW FREQUENCY SWITCHING NOISE SUPPRESSION IN MULTILAYER PRINTED CIRCUIT BOARDS USING A CHIP CAPACITOR LATTICE

BACKGROUND

[0001] This invention is related generally to reduction of noise induced in power planes due to switching of digital circuits in multilayer printed circuit boards. More particularly, the present invention is related to circuits and method for suppression of transverse electromagnetic modes in parallel plate waveguides.

[0002] A common problem in electronic systems is switching noise induced in the power distribution system by the operation of digital circuits in the system. Conventionally, such a system has one or more power planes designated, for example, +Vcc, and one or more ground planes. The potential difference between the power plane and the ground plane provides operating voltage for the circuits of the system. If the system includes digital or other circuits with fast-switching outputs, noise can be induced in the power planes and even in the ground plane. The noise may have several sources, but generally is due to the high slew rate of the digital output and the non-zero inductance of the power plane. Especially for an output driving a large capacitive load, the $L(di/dt)$ noise can be substantial. This noise on the power plane can affect other circuits, slowing system operation or producing data errors. The problem occurs in all types of systems, including integrated circuits and circuits formed on printed circuit boards (PCBs).

[0003] One of the techniques to mitigate power plane noise induced by digital switching uses radio frequency (RF) bypass capacitors between +Vcc and ground layers. Other techniques use a very thin high dielectric constant material between the parallel-plate waveguides for power distribution or split power planes which meet at only one common point.

[0004] The use of board-mounted bypass capacitors is the standard noise suppression approach. The idea of this approach is to provide a very low reactance path between power and ground to decouple high-frequency signals (noise) from the power terminal of a switching device such as a digital IC. To this end, capacitors of widely different values (lower values have less parasitic

inductance) are placed as close as possible to the power pins of integrated circuits. These capacitors are scattered and distributed only in a few locations where large integrated circuits such as the microprocessor exist.

[0005] Depending on the application, this approach may be adequate to reduce the power plane noise problem to an acceptable level. However, as the circuitry in electronics utilize higher frequencies, scattered capacitors will not be able to serve designs in the future.

[0006] The use of very thin (~ 2 mil) dielectric cores, such as Nelco 4000-13 BC or ZBC 2000™ from Merix Corp., Forest Grove, Oregon, to separate power and ground planes helps to decouple RF signals so that the required number of decoupling capacitors may be reduced. This approach is called a buried capacitor layer. However, it will not suppress the parasitic resonance of parallel plate modes because it will not cut off transverse electromagnetic (TEM) modes.

[0007] Subdividing the power and/or ground planes into multiple smaller planes connected only at one point will help to isolate digital noise and raise the frequency of parasitic resonances, but it will not eliminate the power plane noise problem. There are also practical limits as to how small or narrow power or ground planes can be made. As the conductors become narrower, the self inductance of the traces can create noticeable voltage drops due to $L(di/dt)$ when fast switching occurs for high current loads. Also, narrow necks in the power or ground planes can cause heating due to resistive losses or complete breakdown at sufficiently high current levels.

[0008] One reference (Kamgaing, 2002) has described a parallel plate waveguide which has a lower plate formed by an electromagnetic bandgap structure. While the disclosed device has some desirable features, the overall thickness of the disclosed parallel plate waveguide is more than 4.5 mm. For modern printed circuit board applications, this dimension is far too large for practical application. A much thinner parallel plate waveguide is required for integration as a power distribution system in a PCB.

[0009] In addition, it is desirable to have as wide a stopband as possible. The stopband is the range or band of frequencies over which noise and electromagnetic coupling are suppressed or attenuated. It is also desirable to have

the lower edge of the lowest stopband attenuate signals at low frequencies (below a few hundred MHz or less).

[0010] Accordingly, there is a need for improved circuits, devices and methods for reducing induced power plane noise and improving electrical isolation between the various chips sharing a power distribution network (PDN).

BRIEF SUMMARY

[0011] By way of introduction only, the present embodiments provide a two-dimensional, periodic, metallo-dielectric structure, which acts as a distributed microwave bandstop filter integrated into a parallel-plate waveguide. These embodiments can be used as an electromagnetic interference (EMI) filter to suppress digital noise on power planes, as well as to eliminate power plane resonances. Hence, they may be used for EMI and EMC (electromagnetic compatibility) purposes in printed circuit boards. The periodic structures disclosed herein have electromagnetic stopbands and passbands for TEM-like modes that propagate in parallel-plate waveguides. Therefore, these structures share characteristics of electromagnetic bandgap (EBG) filter concepts. The embodiments described herein extend the lower edge of the fundamental (i.e. lowest frequency) stopband of similar reference structures to well below several hundred MHz.

[0012] In other disclosures, periodic structures containing buried patches capacitively coupled to an upper plane and connected to a lower plane through vias were shown to cut off noise over frequency bands at which decoupling capacitors fail. Example designs implemented with printed circuit board (PCB) technology were shown to have a lower frequency cutoff of 1 to 2 GHz and an upper frequency cutoff between 5 and 10 GHz. The lower frequency cutoff is limited by the capacitance of the parallel plates formed by the buried patch and the upper conducting plane. If a much greater value of capacitance were used, the lower cutoff frequency would be decreased without increasing the thickness of the overall structure. Alternatively, the lower stopband frequency could be reduced by increasing the inductance of the vias. However, this is not usually desirable since it leads to a smaller stopband bandwidth. Increasing the via

inductance may be accomplished by decreasing the via diameter, which adds cost, or increasing the length of the via, which adds to the board thickness. Thus, the preferred way to decrease the lower cutoff frequency is to increase the capacitance within each unit cell in the periodic structure.

[0013] Although surface mount technology (SMT) capacitors are relatively inexpensive to add to a PCB design, several problems exist with the placement of only a few scattered capacitors around a chip. Isolated capacitors have practical high frequency limits of about 1 GHz or less due to the parasitic series inductance of vias used to connect the bypass capacitor between +Vcc and ground layers. Also, apart from the vias, the parasitic inductance inherent in the capacitors reduces the high frequency limit of operation.

[0014] In particular embodiments, a new structure may be formed as part of a PCB power distribution network to reduce noise coupled from digital switching circuits to power and ground planes of the PCB. With current PCB technology, only a limited amount of capacitance can be realized with parallel plates. For example, a square parallel plate capacitor with sides of 250 mils that are separated by a dielectric material having a thickness of 2 mils and dielectric constant of 4.3 has a capacitance of 30 pF. Use of conventional SMT chip capacitors with much greater values of capacitance (e.g., 500 pF, 1800 pF, or more) that are connected with vias between the buried patches and the upper conducting plane increases the overall capacitance of the structure. The vias connecting the buried patches to the ground plane are actually extended toward the upper plane and are connected to the upper plane through the SMT capacitors. The addition of an SMT capacitor in substantially every cell of the structure enables the lower cutoff frequency of the fundamental stopband to be extended below 50 MHz.

[0015] In another embodiment, conductive vias are disposed between the upper and lower planes. An array of capacitors connects the vias on the upper layer to the conductive surface of the upper layer. On the lower layer, the same vias are directly connected to the conductive surface of the lower layer. In one example of this embodiment, the periodic arrays of capacitors of the same value without buried patches extend the high frequency cutoff of the same isolated capacitor. Three 1800 pF capacitors used in this experiment together have a

measured self-resonant frequency of 125 MHz when connected to the power plane through vias of diameter 40 mils and length 30 mils and are not useful for decoupling above 200 MHz. These same capacitors when placed within a periodic array provide electromagnetic decoupling on the power planes to a maximum frequency of 4 GHz. Thus, the maximum frequency of decoupling has been extended by a factor of 20 simply by utilizing the inherent properties of the periodic lattice of capacitors.

[0016] By providing an array of capacitors and tailoring the characteristics of the capacitors in a regular or near regular lattice (i.e. periodic or nearly periodic structure), as well as the vias and any patches that may be present in the various structures, the structure may be optimized to produce a stopband in which TEM mode propagation is suppressed over desired frequency ranges including an enhanced low frequency stopband.

[0017] Adding an array of conventional SMT capacitors to a noise-mitigating structure containing an array of buried patches can extend the low-frequency cutoff from 1 to 2 GHz to 50 MHz or less. Therefore, cutoff may be realized from very low in frequency to 10 GHz using arrays of buried patches with arrays of SMT capacitors.

[0018] Thus, an isolated capacitor is useful for decoupling noise from power planes up to a maximum frequency of 100 - 500 MHz, depending upon the capacitance of the capacitor. An array of similar SMT capacitors even without buried patches extends the upper frequency cutoff of an isolated capacitor to much higher frequencies, such as 3 to 4 GHz in examples shown here. This example elucidates the power of lattice structures for exhibiting electromagnetic bandgap performance that is not evident from the individual components comprising the lattice. Thus, embodiments comprising arrays of buried patches and SMT capacitors offers significantly improved suppression of electromagnetic coupling and switching noise in power distribution networks over what has been attainable in conventional designs using isolated bypass capacitors alone or structures consisting of buried patches alone.

[0019] The foregoing summary has been provided only by way of introduction. Nothing in this section should be taken as a limitation on the following claims, which define the scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Fig. 1 is a cross-sectional view of a first embodiment of a parallel plate waveguide with buried patches and SMT capacitors;

[0021] Fig. 2 is a top view of an embodiment of the parallel plate waveguide illustrating the lattice of SMT capacitors;

[0022] Fig. 3 is a cross-sectional view of the structure of Fig. 1 embedded within a PCB with signal layers on the top and bottom.

[0023] Fig. 4 is a top view of the embodiment of Fig 3.

[0024] Fig. 5 is a cross-sectional view of the structure of Fig. 1 with the buried patches removed.

[0025] Fig. 6 is a cross-sectional view of the structure of Fig. 5 embedded within a PCB with signal layers on the top and bottom.

[0026] Fig. 7 is a cross-sectional view of an embodiment of the parallel plate waveguide having a lattice of SMT capacitors connected with plated through holes.

[0027] Fig. 8 is the structure of Fig. 7 with SMT capacitors mounted on the top and bottom of the PCB frequency.

[0028] Fig. 9 shows a transmission line equivalent circuit model of a unit cell of the embodiment of Fig. 1;

[0029] Fig. 10 shows a transmission line equivalent circuit model of a unit cell of the embodiment of Fig. 5;

[0030] Fig. 11 is a graph of the attenuation per unit cell for the embodiment of Fig 1 calculated from a periodic wave propagation model;

[0031] Fig. 12 is a graph of the attenuation per unit cell for the embodiment of Fig 5 calculated from a periodic wave propagation model;

[0032] Fig. 13 shows the calculated coupling between probes separated by 10 cells of the embodiment of Fig. 1 using the equivalent circuit of Fig 9 for each cell;

[0033] Fig. 14 shows the calculated coupling between probes separated by 10 cells of the embodiment of Fig. 5 using the equivalent circuit of Fig 10 for each cell;

[0034] Fig. 15 shows the top view of the hardware implementation of Fig. 2 with three ports labeled as illustrated.

[0035] Fig. 16 shows the bottom view of Fig 15 with SMA connectors at the port locations.

[0036] Fig. 17 is a cross sectional view of the PCB stackup of the hardware of Figs 15 and 16;

[0037] Fig. 18 is a cross sectional view of the PCB stackup of a baseline parallel plate waveguide structure;

[0038] Fig. 19 shows the measured coupling between ports in the hardware of Fig 15 compared to a baseline parallel plate waveguide of Fig 18;

[0039] Fig 20 shows the measured coupling between ports having the same layout of Fig 15 for the embodiment of Fig 5 with SMT capacitors only compared to the baseline case over the frequency span 50 MHz to 1 GHz;

[0040] Fig. 21 shows the measured coupling between ports having the same layout of Fig 15 for the embodiment of Fig 5 with SMT capacitors only compared to the baseline case over the frequency span 50 MHz to 10 GHz;

[0041] Fig. 22 shows a comparison of measurements of the three cases: SMT capacitors only, buried patches only, and SMT capacitors combined with buried patches ;

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

[0042] Applications, such as those in U.S. Patent Application Serial No. _____ filed, entitled "Circuit and Method For Suppression of Electromagnetic Coupling and Switching Noise in Multilayer Printed Circuit Boards," (hereinafter referred to as reference [1]) which claims priority to Provisional U.S. Patent Application Serial No. 60/477,152 filed June 9, 2003, entitled "Circuit and Method For Suppression of Transverse Electromagnetic Modes," and concurrently filed U.S. Patent Application Serial No. _____ entitled "Circuit and Method for Broadband Switching Noise Suppression in

Multilayer Printed Circuit Boards Using Localized Lattice Structures," all of which are hereby incorporated herein in their entirety by this reference, have focused on two dimensional lattices of buried patches and SMT capacitors and combinations thereof. The term lattice and array are interchangeable throughout this disclosure. The various arrangements in these applications (containing differing patch and via characteristics) may be incorporated as desired into the arrangements shown in the present application.

[0043] Switching of electronic devices such as microprocessors present on a PCB introduces noise in the power distribution network. The noise introduced has a fundamental frequency and harmonics related to the switching frequencies of the electronic devices, the materials and geometries used in the design of the PCB structure and other factors. Preferably, the features of the TEM mode suppression circuit disclosed herein are chosen to suppress or limit this noise. More particularly, the fundamental stopband of the TEM mode suppression circuit should be designed to suppress propagation of the TEM modes at frequencies of interest, e.g. the switching frequencies of the electronic devices. In this manner, noise introduced at a noise source in the power distribution network on either the positive voltage node or the ground node is significantly attenuated at other digital devices or other components of the PCB.

[0044] The embodiments described herein attenuate parallel-plate TEM modes that are naturally guided between the parallel conductive surfaces shown in Fig. 1. TEM modes are guided waves moving transverse or across the inside surface of the PPW, in parallel with the plane of the PPW. As shown in FIG. 1, the metal or other conductor planes lie parallel to the x-y plane. A TEM mode has a normal (z-directed) electric field and a transverse (x-directed) magnetic field, assuming wave propagation in the y direction. An empty parallel-plate waveguide (PPW) allows the TEM mode to propagate from DC to an infinite frequency. In this context, an empty PPW is one with no electromagnetic bandgap (EBG) structure. There exists no inherent cutoff frequency for TEM modes in an empty PPW.

[0045] The present embodiments create one or more stopbands of frequencies over which TEM modes do not propagate within a PPW. Hence these

embodiments may be referred to as TEM mode suppression circuits. Frequency ranges in which the attenuation is substantially less than (30 dB or so) that in the stopband will be called passbands.

[0046] Referring now to the drawings, FIG. 1 illustrates a first embodiment of a parallel plate wave guide (PPW) 100 containing a transverse electromagnetic (TEM) mode suppression circuit. FIG. 1 is a cross-sectional view of the PPW 100. The PPW 100 includes a lower metal layer 102, an upper metal layer 114. Disposed a distance t_2 from the upper metal layer is a third metal layer 108 which forms buried patches. Metal layers 108 and 114 are separated by a dielectric layer 110 of thickness t_2. Metal layers 102 and 108 are separated by a dielectric layer 106 of thickness t_1. An array of conductive rods 104 of length $t_1 + t_2$ and radius a extend between the lower layer 102 and the upper layer 114. Unless otherwise noted, the dimensions shown in the figures do not include the thickness of the conductive surfaces, which may be a relatively thin metal. The conductive rods may be solid metal poles or may be plated through holes (vias) whose edges are coated with metal but whose centers remain empty. The conductive layer 114 is a metal pattern that extends over substantially the entire top surface area of the upper layer, with openings for the conductive rods such that the only physical contact between the metal of the conductive rods and the metal of the conductive portion on the top surface of the upper layer is through the capacitors 116.

[0047] The period of the patches is generally the same as the period of the conductive rods and SMT capacitors, but may be different. Similarly, while the patches and capacitors usually exist in a one-to-one correspondence with each other such that each patch is associated with a capacitor, this is not necessary; particular areas of the board do not permit either patches or capacitors to be present. Although in general substantially the same number of the patches and capacitors are provided, quantification of the ratio is highly dependent on the design layout of the PCB. Similarly, although the lattice of capacitors generally are disposed over the entire surface area of the PCB/various layers, because the number and type of electronic components vary dependent on the board design and other requirements, absolute quantification of the overall coverage of the PCB by the lattice is likewise dependent. The patches 108 are much larger than

the conductive rods 104. The patches 108 overlap with the conductive upper layer 114 to create parallel-plate capacitors in parallel with the capacitors 116.

[0048] The diameter of the conductive rod is, for example, 40 mils and the overall thickness of the PPW 100 is about 30 mils. Thus, Fig. 1 is not illustrated to scale. The conductive rods may, but are not required to, penetrate the entire height of the PCB structure. The thicknesses of the first dielectric layer 106 and second dielectric layer 110, for example, are 24 mils and 3 mils, respectively. The length of the conductive rods 104 in this example is the same as the total thickness of the PPW 100: 30 mils. The first dielectric layer 106 may be formed of any dielectric material such as RO5880 or FR4 with copper on both sides to form layers 102 and 108. Layer 108 is then etched using standard PCB processing techniques to create the buried patches. The upper dielectric layer 110 can be comprised of a thin FR4 or other dielectric material with copper on one side (114) and is attached to the lower dielectric 106 with a bonding film that is sometimes referred to as prepreg. Thus, the dielectric layer 110 may include both the laminate material (FR4) and the bonding film, both of which are dielectrics.

[0049] The combination of double clad and single clad dielectric sheet materials with prepreg bonding films comprise a specific stackup of a PCB design. Many combinations of stackups are possible to achieve a given cross section. The description of the stackup in Fig. 1 is exemplary only and does not limit the scope of the invention.

[0050] Sections 105 of the surface of the upper conductive layer 114 house ends of the conductive rods 104. More specifically, at the periphery of each conductive rod 104, a pad 105 is formed to terminate the conductive rod 104 on the upper surface of the PCB 100. To avoid a short circuit, a clearance space 113 is provided around the conductive pad 105 by etching or some similar means. The clearance space and the diameter of the pad in the embodiment shown in Fig. 1, for example, are preferably kept to a minimum to maximize the capacitance between the patches and the conductive surface of the upper layer.

[0051] Capacitors 116 (in one embodiment SMT capacitors such as 1800 pF, 50 VDC capacitors made by Panasonic, Digi-Key P/N PCC2157CT) connect the ends of the conductive rods 104 and pads 105 with the conductive upper layer

114. The capacitors 116 add additional capacitance to the structure, compared to structures containing only patches. The chip capacitors may also include non-SMT type capacitors.

[0052] The conductive rods 104 are oriented generally normal to both the lower layer 102 and the upper layer 114. Each respective conductive rod 104 is in electrical contact with the lower layer 102 and with a respective capacitor 116. In some embodiments, each plated through hole has an associated capacitor while in other embodiments, some of the capacitors or capacitors and conductive rods may be omitted so that there is not a one-to-one correspondence between conductive rods and capacitors.

[0053] The conductive rods 104 and capacitors 116 in the embodiment of Fig. 1 are arrayed in a square lattice of period d (for example, 250 mils). Various structures and reasons for using lattices are provided in U.S. Patents 6,512,494 and 6,262,495 herein incorporated by reference in their entirety. In general, any two dimensional lattice consisting of arbitrary direction vectors and spacing may be used. The first and second dielectric layers 106, 110 form the host dielectric medium of the PPW 100. The first (lower) dielectric layer 106 of thickness t_1 has a relative dielectric constant of ε_{r1}, while the second (upper) dielectric layer 110 has a relative dielectric constant of ε_{r2}. One example of materials used for the lower dielectric layer includes RO5880, which has a dielectric constant of 2.5. An example for the upper dielectric layer is FR4, which has a dielectric constant of 3.9. In order to maximize the stopband bandwidth, the relationships between these thickness and dielectric constants should be $t_2 < t_1$ and $\varepsilon_{r2} \geq \varepsilon_{r1}$.

[0054] The dielectric layers 106, 110 are normally isotropic. However, as only the normal or z-directed tensor component of permittivity affects the electric field of the TEM mode, if anisotropic dielectric materials are used for the layers 106 and 110, then the z tensor element can be substituted for the relative dielectric constant.

[0055] Fig. 3 illustrates a cross-section view of the noise suppression circuit of Fig. 1 embedded within a multilayer PCB. In this embodiment, dielectric layers 318 and 320 are added to the top and bottom of the parallel plate structure of Fig 1. In this example, metal layers 324 and 322 are used to route signals to

various chips on the board. Layer 314 is used as the Vcc plane, and layer 302 is used as the ground plane. The vias 304 connect the patches 308 and the capacitors 316 to the ground plane 302 through the dielectric layers 306, 310, 318. The vias 326 connected the capacitors 316 to the Vcc plane 314 through the dielectric layer 318. Fig 4 illustrates a top view of this configuration showing that each lead of a given capacitor 416 is connected to vias 404, 426 which extend into the PCB 400.

[0056] In some applications, the buried patches may be eliminated and the noise suppression circuit becomes a periodic lattice of SMT capacitors only, as illustrated in Fig. 5. This embodiment is the same as that of Fig. 1 with the buried patches removed. The vias 504 connect the capacitors 516 to the ground plane 502 through the dielectric layers 506, 510. Pad 505 is again separated from the metal layer 514 by a clearance space 513.

[0057] Figure 6 shows the embodiment used within a multilayer printed circuit board 600. In this example, vias 604 and 626 connect the SMT capacitors to the ground plane 602 and Vcc plane 614, respectively. In this embodiment, dielectric layers 618 and 620 are added to the top and bottom of the parallel plate structure of Fig 1. In this example, metal layers 624 and 622 are used to route signals to various chips on the board. The vias 604 connect the capacitors 616 to the ground plane 602 through the dielectric layers 606, 610, 618. The vias 626 connected the capacitors 616 to the Vcc plane 614 through the dielectric layer 618.

[0058] Figure 7 shows an example of the periodic lattice of SMT capacitors in which plated through holes penetrate the PCB 700 and connect to the Vcc plane 714 and ground plane 702. In this example, only one dielectric layer 706 is used to separate the Vcc plane 714 and ground plane 702 since there are no buried patches. The signal layers 722, 724 contain traces that carry digital transmissions between various chips and also make connections to discrete components. The vias 704 connect the capacitors 716 to the ground plane 702 through the dielectric layers 706, 718 and extend to ground traces on the bottom signal layer 722 through the dielectric layer 720. Similarly, the vias 726 connected the capacitors 716 to the Vcc plane 714 through the dielectric layer 718 and extend to ground

traces on the bottom signal layer 722 through the dielectric layers 706, 720. As in the other embodiments, clearance spaces 713 are formed between the vias and the metal of the other layers through which they pass (e.g. Vcc plane 714 for via 704 and ground plane 702 for via 726).

[0059] In the embodiment of Fig. 8, SMT capacitors 816 and 828 are located on both sides of the PCB 800 and are connected to the Vcc plane 814 and the ground plane 802 through vias 804 and 826. Again, only one dielectric layer 806 is used to separate the Vcc plane 814 and ground plane 802 since there are no buried patches. The signal layers 822, 824 contain traces that carry digital transmissions between various chips and also make connections to discrete components in addition to the capacitors 828. Dielectric layer 820 separates the ground plane 802 from signal layer 822, while dielectric layer 818 separates the Vcc plane 814 from signal layer 824. This configuration yields more capacitance per unit cell than those having a capacitor on only one side of the board. Alternatively, the embodiment 800 allows greater flexibility in the PCB layout since capacitors may be removed on one side of the board in order to make room for chips while still remaining on the opposite side of the board for improved noise suppression.

[0060] Of course, in any of the above embodiments, geometries other than square lattices may be used to create the array (e.g. hexagonal or triangular lattices) so long as waves of electromagnetic energy at the desired frequencies are attenuated between the points of interest.

[0061] Fig. 9 illustrates a transmission line circuit model of one unit cell of the low frequency enhanced noise suppression circuit of Fig. 1. In this circuit model, the capacitance C1 is the parallel plate capacitance formed by the buried patches 108 and the upper conducting plane 114. L1 is the inductance of section of the via 104 that extends from the ground plane 102 to the buried patch 108. L2 is the inductance of the section of the via 104 that extends from the buried patch 108 to the upper conducting plane 114. C2 is the capacitance of the SMT capacitor that is connected between the via pad 105 and the upper conducting plane 114. Figure 10 illustrates a transmission line circuit model of one unit cell of the low frequency enhanced noise suppression circuit of Fig. 5. In this model,

the capacitance of the buried patch C1 is removed. The remaining circuit elements used to create the stopband are L1 and L2 which together represent the inductance of the vias 504 and C2 which is the capacitance of the SMT chip capacitor. It is recognized that this circuit model for the unit cell is the same as the one described in reference [1]. However, in this case, the value of capacitance is much larger since SMT chip capacitors are used. Later, it will be shown that this leads to significant improvement at frequencies below 1 GHz. These circuit models of one unit cell can be used to predict the electrical performance of the low frequency enhanced noise suppression embodiments. Component values shown in Figs. 9 and 10 are exemplary only and depend upon specific design requirements as described later.

[0062] The equivalent circuits in Figs. 9 and 10 are referred to as transmission line equivalent circuits (TLEC) and can be used in two ways. First, as described in detail in reference [1], analysis of an infinite periodic structure of identical TLECs will result in an $\omega\beta$ diagram or dispersion diagram. Also, this method is used to generate plots of attenuation per unit cell. Second, a more convenient use of the TLEC is to chain a finite number of these cells together and analyze the resulting finite structure with a commercially available circuit simulator (such as Eagleware's Genesys). This second approach results in plots of S12 versus frequency.

[0063] Both cases of the low-frequency enhanced structures of Fig. 1 and Fig 5 were modeled with the methods discussed above and were later fabricated and tested. The various circuit elements describing the unit cells in Figures 9 and 10 may be calculated from the geometry of the structure. In the unit cell of Figs. 1 and 3, the patches are squares having a 230-mil side length (s) and a 20-mil spacing (g) between the patches. Thus, the period (d) of the array of patches is 250 mils. The first dielectric layer (t_1) is 24 mils thick and has a relative dielectric constant (ε_{r1}) of 2.5, the second dielectric layer (t_2) is 3 mils thick and has a relative dielectric constant (ε_{r2}) of 3.8, each conductive rod has a radius a of 20 mils, and the capacitance (C_2) of each chip capacitor is 1800 pF. The capacitance (C_1) of the buried patches is calculated from the parallel plate capacitance formula ($C_1=\varepsilon_{r1}\varepsilon_0 s^2/t_2$) to be around 14.7 pF. The inductance of each conductive

rod from the lower layer to the layer of patches (L_1) is 0.29 nH, while the inductance from the layer of patches to the chip capacitor (L_2) is 0.155 nH. Expressions for calculating the inductance per unit length of a single rod embedded within a periodic structure of rods having period d is discussed in reference [1]. These expressions were used as a guide for determining the values of L_1 and L_2. The values used for L_1 and L_2 were varied so that the calculated results would more closely match the measured results presented later. The impedances (Z_0) of the transmission line sections are calculated to be 25.2 Ω while the effective dielectric constant $(\varepsilon_{r1} \times t_1 + \varepsilon_{r2} \times t_2)/(t_1 + t_2)$ is 2.6. These transmission line sections are of half the length of the period d.

[0064] Figure 11 shows the attenuation per unit cell for the TLEC illustrated in Fig. 9. This prediction illustrates that the first fundamental stopband exists over the frequency range 130 MHz to 3 GHz. A second stopband is predicted to occur over 4 – 8 GHz, and a narrow passband is predicted to exist over 3 – 4 GHz. When the capacitor C1 is removed from the TLEC in Fig. 9 resulting in the circuit model of Fig. 10, then the predicted frequency response is as illustrated in Fig. 12. This calculated result for the structure having SMT capacitors without buried patches shows a stopband over the frequency range 130 MHz – 6 GHz.

[0065] Fig. 13 is the calculated coupling data of two 50 Ohm ports with ten unit cells of Fig. 9 cascaded between them. This data indicates that a passband occurs between 3 and 4 GHz and stopbands occur between 150 MHz – 3 GHz and 4 GHz – 7.5 GHz. These results are very similar to the attenuation per unit cell data of Fig. 11. When the capacitance of the buried patches is removed from the circuit model, the coupling data of Fig. 14 is predicted. In this case, the stopband of 150 MHz – 5.5 GHz is in good agreement with the calculated stopband in Fig. 12.

[0066] Hardware was fabricated in order to test the performance of the embodiments described in Figures 1 and 5. The top view of the hardware is shown in Fig. 15 and is representative of both embodiments with and without buried patches since the inside metal layer forming the patches cannot be viewed. SMT capacitors are soldered within each unit cell as described previously and are shown in the inset of Fig. 15. Three SMA connectors were soldered to the PCB

and centered on drilled-out vias as shown in Figures 15-16. The center conductor for each connector was soldered to the upper conductive surface of the PPW and the outer conductor was soldered to the lower conductive surface of the PPW so as to excite or receive TEM modes. The PCBs contained 17 x 21 cells (4.25 inches x 5.25 inches). As can be seen in Fig. 16, only the SMA connectors (i.e. no chip capacitors) were installed on the base of the PCB by soldering. The second and third SMA connectors were disposed along a horizontal line with 10 unit cells between them, while the first and third SMA connectors were disposed along a line 45° from the horizontal line with 7 unit cells (with or without patches or SMT capacitors) between them. The connectors were located in these positions in order to test the effects of coupling paths that are not aligned with the axes of the lattice structure. Each connector was located at least 4 unit cells from the nearest edge. Again, the materials and geometries are exemplary only.

[0067] The PCB stackup for implementing the embodiment of Fig. 1 in hardware is shown in detail in Fig. 17. The PCB 1700 contains a first dielectric region 1706 made of R05880 material which is a Teflon-based dielectric manufactured by Rogers Corporation, One Technology Drive, Rogers, CT 06263-0188. This dielectric material is 20 mils in thickness (t_1) and is clad with copper only on the bottom side to form the lower conducting plane 1702. A second dielectric material 1712 is 3-mil thick (t_2) FR4 with copper on both sides that forms the upper conducting plane 1714 and the buried patch layer 1718. After the copper of the second dielectric layer 1712 is etched on both sides with the appropriate artwork pattern, the two dielectrics 1706, 1712 are joined with a bonding material 1708 that is also referred to as prepreg which is 4 mils in thickness (t_3). The prepreg material is an epoxy loaded with woven glass fiber. The resulting stackup is pressed together under heat and pressure so that the prepreg 1708 will bond the two laminate layers together. The finished PCB 1700 has a total thickness of 30 mils. The structure 1700 is drilled and plated to form the conducting via 1704 that connects a pad 1705 on the upper surface to the buried patch 1718 and ground plane 1702. The pad 1705 is separated from the remainder of the upper conducting plane 1714 by a clearance space 1713. The diameter of the vias 1704 is 40 mils. In this case, 1800 pF SMT capacitors 1716

are soldered between the via pad 1705 and the upper conducting plane 1714. For the case in which no buried patches are present, the upper dielectric material 1712 has copper on only one side for the upper conducting plane 1714 and the other copper layer 1718 is completely removed.

[0068] In order to demonstrate the improvement that is achieved when the noise suppression circuits are used, a baseline PPW was fabricated according to the stackup of Fig. 18. Essentially this is the same stackup as Fig. 17 with the buried patches, SMT capacitors, and vias removed. The stackup 1800 includes a bottom dielectric layer 1806 of R05880 that has one layer of copper 1802 and is 20 mils in thickness (t_1). The upper dielectric layer 1812 is made of 3-mil thick (t_2) FR4 and has copper only on the upper surface 1814. A bonding layer of prepreg material 1808 is of thickness 4 mils (t_3) and is used to adhere the two laminate regions together. Three coaxial connectors (not shown in Fig. 18) are soldered to the baseline board in the same locations as described previously for the other cases.

[0069] Figure 19 is a graph of the measured transmission data of the hardware described in Figs. 15-18. The coupling data for the baseline PPW is provided along with data for the noise suppression circuit embodiment having both SMT capacitors and buried patches. The measurements were performed on an HP8720ES vector network analyzer. The experiment was configured to determine if the coupling of power between the ports depends upon their alignment with the lattice of the periodic structure. In Fig. 15 it is seen that the line between ports 2 and 3 is aligned with an axis of the lattice, whereas the line between ports 3 and 1 is at a 45 degree angle to this axis. Ports 2 and 3 are separated by 9 unit cells and a distance of 2.5 inches. Ports 1 and 3 are separated by 6 unit cells and 2.5 inches. S13 is the ratio of power transmitted to port 1 and power incident from port 3 expressed in decibels. S23 is the ratio of power transmitted to port 2 and power incident from port 3. As is evident in the data of Fig. 19, despite the differences in the alignment of the ports, the transmission characteristics are very nearly the same between the third and second ports (S23) and between the third and first ports (S13). Thus, it is not necessary for the

shortest coupling path between interferers on a printed circuit board to align with the lattice axis in order to get the benefit of noise suppression.

[0070] In Fig. 19, it is seen that the noise suppression circuit containing SMT capacitors along with buried patches attenuates coupling by an extremely large amount, 70 dB or more, over most of the frequency range between 50 MHz and 8.5 GHz. There is less attenuation, about 36 dB, occurring in the 3-4 GHz range. However, the attenuation of coupling over 3-4 GHz is still significant since it is about 20 dB better than the nominal response for the baseline case without a noise suppression circuit. Thus, the effective stopband is essentially from 50 MHz to 8.5 GHz in this example of a noise suppression circuit containing SMT capacitors and buried patches.

[0071] In Fig. 20 and 21, the coupling for the baseline PPW may be compared to embodiments of parallel plate waveguides loaded with SMT capacitors only and without buried patches. The same data is plotted in both figures. However, in Fig. 20 the frequency range is 0 to 1 GHz, and in Fig. 21 the frequency range is 0 to 10 GHz. Fig. 20 shows that three isolated 1800 pF capacitors have a self resonant frequency of 125 MHz when connected to the PPW through conducting vias of diameter 40 mils and length 30 mils. These three capacitors alone are not very useful for decoupling high frequency noise from the power planes at frequencies above 200 MHz since the transmission data approaches that of the baseline PPW at this frequency. However, when the same 1800 pF capacitors are placed in a lattice structure throughout the PCB, significant decoupling occurs up to a maximum frequency of 4 GHz as seen in Fig. 20. Thus, the use of SMT capacitors even without buried patches has extended the upper frequency limit of the stopband of isolated capacitors from several hundred MHz to 4 GHz in this example. The stopband of 50 MHz to 4 GHz in this case covers the low frequency spectrum not addressed by the structures available in reference [1].

[0072] In Fig. 22 the coupling measurements between the first and second ports (S12) for three configurations are compared: SMT capacitors only, patches only, and SMT capacitors and patches. The array of SMT capacitors alone provide the stopband below 4 GHz and the array of patches alone provide the stopband over 3.5 – 8.5 GHz. The array of SMT capacitors in conjunction with

buried patches results in a passband between 2.5 and 4.5 GHz over which the coupling is attenuated significantly less than in the adjacent stopbands. The existence of this passband can be explained by examining the circuit model for the unit cell in Fig. 9. At frequencies above the series resonance frequency of C2 and L2, this branch of the circuit appears inductive. Thus this branch will form a parallel LC resonant circuit with C1 which will appear as an open circuit at the parallel resonant frequency. Within a narrow band around this parallel resonant frequency, the shunt load of C1 in parallel with L2 and C2 will have a high impedance which will allow coupling to occur from one side of the unit cell to the other. Thus, significant noise suppression is not possible at these frequencies using an arrangement that provides a circuit model.

[0073] However, using different component values can change this passband region. This is to say that the passband region may possibly be decreased or eliminated by different combinations of changing the capacitance of the chip capacitors, changing the capacitance formed by the patches (through changing the size of the patches or the dielectric constant between the patches and the conductive surface for example), or changing the different inductances (through changing the size, number, and/or distribution of the vias for example).

[0074] Of course, in addition to the arrangements of the patches shown in the figures, it is possible to use other arrangements, such as those shown in the patent applications incorporated by reference. Rather than present all of the figures and describe them again, a brief summary of some of the arrangements follows.

[0075] Methods of reducing the lower edge of the fundamental stopband for arrays with patches only, one may increase the capacitance of the patches by increasing the dielectric constant of the material between the patches and the conductive surface of the upper layer, increasing the area of the patches, or reducing the thickness between the patches and the conductive surface of the upper layer, increase the height of the PPW, or increase the inductance of the via by decreasing the cross sectional area of the vias. To increase the upper edge of the fundamental stopband one may decrease the period of the array, decrease the effective dielectric constant of the PPW, or increase the inductance of the via by

increasing the cross sectional area of the via and/or providing multiple vias for the same patch.

[0076] Embodiments may be used that adjust the thicknesses and dielectric constants of the dielectric layers, adjust the height of the overall PCB structure, adjust the shapes and sizes of the patches and/or vias, coplanar spirals or meanderlines may be formed to increase the series inductance (L_1) without increasing the period of the array, or multiple levels of capacitive patches may be used to increase the capacitance. The last embodiment may be readily integratable with existing board designs if even numbers of layers of patches are used. This permits addition of an even number of layers to an existing board design and while still maintaining advantages provided by the use of only even numbers of layers in board designs.

[0077] The height of the overall PCB structure may be minimized as in many applications it is desirable to reduce the vertical dimension of a printed circuit board (PCB). Current stack-up dimensions of state-of-the-art computer servers for example may contain five or more pairs of power/ground planes in one PCB. Power system designers attempt to place power and ground planes as close together as possible to obtain the lowest characteristic impedance possible for the power distribution system with typical separation distances of 10 mils or less. Spacing is as close as 2 mils in some cases. This low characteristic impedance minimizes the voltage fluctuations present on a power distribution network (PDN) when transients of supply current are present.

[0078] Inhomogeneous mode suppression structures may be created to create broader frequency stopbands between two different reference plane locations on the same PCB. In these structures, the band edges vary in frequency as a function of lateral position within the PCB because the properties of the unit cell change with location. Non-planar structures such as those curved in cross section (including coaxial or square cross sections) and non-uniform patches and/or vias may also be used.

[0079] From the foregoing, it can be seen that the present embodiments provide improved circuits, devices and methods for reducing induced power plane noise and improving RF isolation. The devices may be embodied as

periodic structures within waveguides capable of supporting TEM mode propagation, or as transverse electromagnetic mode suppression circuits. These embodiments have several distinct advantages over conventional EMI or EMC solutions.

[0080] The embodiments offer significantly more RF isolation than is attainable from discrete bypass capacitors or arrays of patches alone. Isolation levels of 70 dB or more are practical between points on a power plane separated by only 2.5 inches. The disclosed embodiments cut off parallel plate modes that travel in any transverse direction, assuming the power plane is large enough in transverse dimensions to accommodate several periods of cells. These embodiments can readily be designed to have a transmission zero ($L_I C_I$ resonance) as low as 50 MHz or less when SMT capacitors are added to the structure.

[0081] It is therefore intended that the foregoing detailed description be regarded as illustrative rather than limiting, and that it be understood that it is the following claims, including all equivalents, that are intended to define the spirit and scope of this invention. For example, the geometries and material properties discussed herein and shown in the embodiments of the figures are intended to be illustrative only. Other variations may be readily substituted and combined to achieve particular design goals or accommodate particular materials or manufacturing processes.